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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,434	09/05/2003	Hitoshi Yamamoto	2271/70977	8466

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 11/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/656,434	YAMAMOTO, HITOSHI	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 10-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 10-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Serial Number: 10/656434 Attorney's Docket #: 2271/70977
Filing Date: 9/5/2003; claimed foreign priority to 9/6/2002

Applicant: Yamamoto

Examiner: Alexander Williams

Applicant's Amendment filed 9/19/06 to the Applicant's election of Group I (claims 1 and 2, now claims 1, 2 and 10-16), filed 7/15/2004, has been acknowledged.

Claims 3-9 have been canceled.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 2 and 10 to 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sawaya (U.S. Patent # 5,245,215) in view of Sahota et al. (WO 01/54047 A1).

As to claim 1, similar claim 10 and there dependent claims, Sawaya (figures 1A to 15B) specifically figures 1A and 1B show a semiconductor device which integrates a plurality of semiconductor chips **12-1,12-2** into a single package, comprising: a first semiconductor chip **12-2** which includes a plurality of first bonding pads **17** outputting first signals having a first level; and a second semiconductor chip **12-1** which includes a plurality of second bonding pa **17** electrically coupled to a part of the plurality of first bonding pads to receive the first signals having the first level from the first semiconductor chip through the part of the plurality of-first bonding pads and a plurality of third bonding pads **17** which converts the first signals received through the plurality of second bonding pad into second signals having a second level different from the first level and outputs the second signals through the plurality of third bonding pads. Sawaya show the structure and features of the claimed invention as detailed above, but fail to explicitly show a signal level conversion circuit, configured to convert the first signals of the first level into second signals having a second level different form the first level and outputs the second signals and wherein said first level and said second level correspond to respective, different driving voltages in a digital circuit. Since this language is functional limitation that must be evaluated and considered, just like any other limitation of the claim, for what it fairly conveys to a person of ordinary skill in the pertinent art, consideration of function language is acceptable so long as it sets definite boundaries on the patent protection sought. *(See MPEP 2173.05g) In re Bar, 170 USPQ 33 (CCPA 1971).* In consideration of the functional limitations for purpose of applying the prior art, the Examiner, applied the prior art with features of the apparatus

structurally, and did not distinguish from the prior art in terms of structure rather than function alone. *(see MPEP 2114) See In re Swinehart, 169 USPQ 226 (CCPA 1971); In re Schreiber, 44 USPQ2d 1429 (Fed. Cir. 1997).* The Examiner has a reason to believe that the function limitation can be performed by the prior art structure using any given amplifier the structure. The recitation directed to the manner in which a claims apparatus is intended to be used does not distinguish the claimed apparatus form the prior art if the prior art has the capability to so perform. *(See MPEP 2114 and Ex parte Masham, 2 USPQ2d 1647 (1987))* However, Sawaya show the claimed structure of the claimed device. The claimed language referring to the signal level conversion circuit recited the function of the claimed semiconductor chip. Sawaya's semiconductor chip products a signal level. Any device structure can have the level or amplitude signal changed to a desired output level in a signal circuit system with a signal conversion circuit or an amplifier as desired to increase the output signal or volume of a signal. It would be obvious to one of ordinary skill in the art to use any means of signal level conversion circuit or amplifier to make the signal output different from the input signal.

Nevertheless, Sahota et al. is cited for showing circuit for providing interface signals between integrated circuits. Specifically, Sahota et al. (figures 1 to 6) discloses circuitry that generates an interface signal between a first and a second integrated circuit, the circuitry comprises a reference circuit that provides a reference signal, an interface circuit, and a circuit element; wherein the interface circuit is implemented on the first IC, operatively coupled to the reference circuit, receives the reference signal and a data input, and generates the interface signal, wherein the circuit element is

implemented on the second IC, operatively couples to the control circuit, receives the interface signal, and provides an output signal, wherein the reference signal can be a voltage or a current signal and can be generated in the first or second IC, where the interface circuit can be implemented with a current mirror coupled to a switch array and can be oversampled to ease the filtering requirement, wherein the interface signal can be a differential current signal for the purpose of providing interface signal that have differential current signal havir multiple bits of resolution and providing interface signals between integrated circuits.

2. The semiconductor device as defined in Claim 1, the combination with Sawaya show wherein the second level is greater than the first level.

Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to use Sahota et al.'s signal level conversion circuit to modify Sawaya's single package for the purpose of providing a display diver for the purpose of providing interface signal that have differential current signal having multiple bits of resolution and providing interface signals between integrated circuits.

Claims 17 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response

Applicant's arguments filed 9/19/06 have been fully considered, but are not found to be persuasive in view of the outstanding modified grounds of rejections detailed above.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., wherein a first semiconductor chip operates with a first driving voltage at a first level in a digital circuit, and a second semiconductor chip includes circuits which operate with a second level corresponding to a second driving voltage in an digital circuit) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Accordingly, **THIS ACTION IS MADE FINAL**. See M.P.E.P. ∋ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. ∋ 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. ∋ 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

The listed references are cited as of interest to this application, but not applied at this time. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Any signal can be amplified in a circuit device.

Field of Search	Date
U.S. Class and subclass: 257/685,723,666,777,686,728,676,678,787,784,786,696, 698,691,690,e23.034,e23.052,e23.124	9/14/04 4/7/05 6/11/06 11/18/06
Other Documentation: foreign patents and literature in 257/685,723,666,777,686,728,676,678,787,784,786,696, 698,691,690,e23.034,e23.052,e23.124	9/14/04 4/7/05 6/11/06 11/18/06
Electronic data base(s): U.S. Patents EAST	9/14/04 4/7/05 6/11/06 11/18/06

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
11/18/06

Primary Patent Examiner
Alexander O. Williams